Chip Design Sign-Off For Shrinking Technology

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***Abstract*-In today's IC's competitive market place, as technology is shrinking and we are stepping into 45nm and below, IC's complexity is increasing, die areas are also getting larger in order to incorporate the increased functionality that comes with more advanced technology. Due to shrinking design, physical verification of design such as design rule checking (DRC) and layout vs. schematic (LVS), may not give accurate result as expected due to electrical side effects inherent in nanometer process technology. Therefore, shrinking designs demand additional verification before being signed-off for manufacturing. For example, if signal integrity (SI) and other electrical effects are not controlled, a design will likely suffer from lower performance, lower yield, and even functional failure. Any chip failure after manufacturing will result in expensive mask changes and delays in getting the chip to market. Consequently, most designs today require a nanometer sign-off process, where the influence of different electrical effects on the functionality and performance of the design are analyzed before manufacturing.**

I. COMPLEXITY DUE TO SHRINKING DESIGN

Implementing 45nm and below design raises significant SI (Signal Integrity) related issues that have to be verified in order to avoid chip functional failure. These include reduced feature sizes, decreases in wire pitch, lower power supply voltages, and shrinking threshold voltages. With each new process technology, more and more levels of wire are packed more closely together. As a consequence, the fraction of total wire capacitance represented by lateral coupling increases dramatically. This in turn is responsible for a dramatic increase in on-chip crosstalk noise. Another electrical problem in shrinking designs is increased clock frequencies with faster on chip slew rates. Faster slew rates create more switching noise and increase instantaneous power consumption. This in turn puts stress on the power grid, resulting in voltage (IR) drop and electro-migration. Nanometer sign-off is becoming a challenge, uncovering any problems that may have been missed during design implementation or that have been caused by last-minute manual design changes.

Nanometer sign-off is a final verification to assure that a design does not have electrical issues that will result in chip failure after manufacture. However, finding many problems only just before manufacturing could lead to multiple design iterations and delay in manufacturing and market.

As design is shrinking, we can observe increased power density, increased clock frequencies and slew rate, lower supply voltage, domination of wire to wire coupling capacitance over ground capacitance, smaller transistor thresholds to decrease transistor delay and because of all these factors we can see from figure 1 that crosstalk glitches are increasing and it gives result of silicon respins, longer design cycle, lower performance and lower yield.

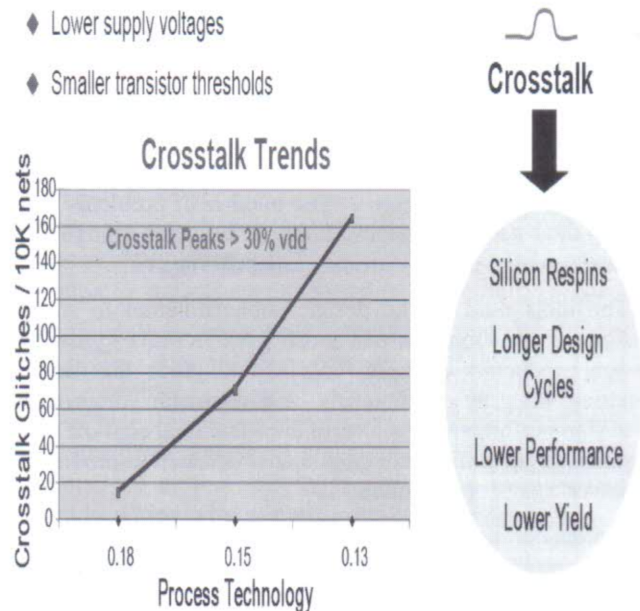

Fig. 1 Crosstalk Trends

II. SHRINKING DESIGN SIGN-OFF REQUIREMENTS

The role of nanometer sign-off is to uncover any problems that may have been missed during design implementation or that have been caused by last-minute manual design changes. Nanometer sign-off is a final verification to assure that a

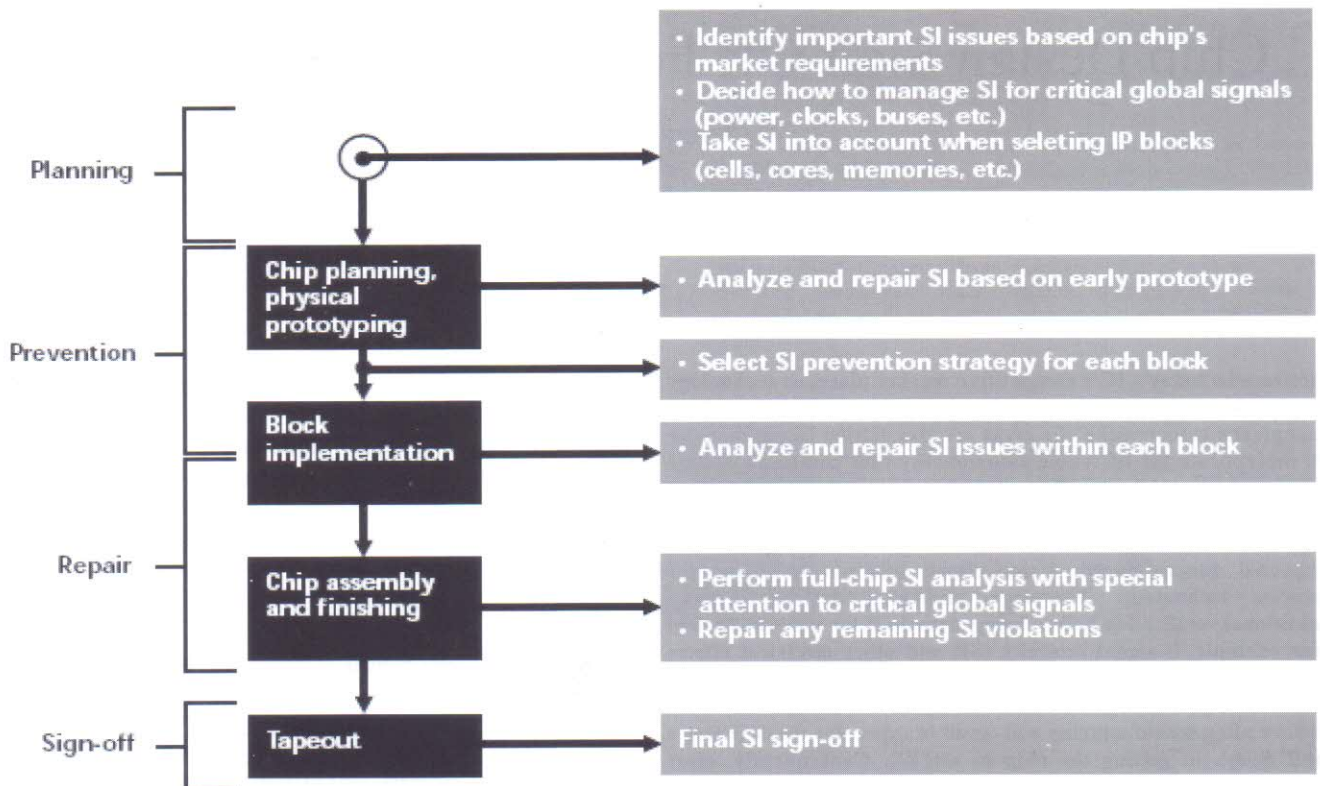

Fig. 2 Flow to fix signal integrity.

design does not have electrical issues that will result in chip failure after manufacture.

45 nanometer and below sign-off is best applied as part of a thorough design closure methodology that issues such as signal and power integrity from early chip planning through to tapeout, as shown in figure 2. The number of problems found during final nanometer sign-off should be small enough to be dealt efficiently, even by means of manual repair.

The tools used during design implementation to support design closure should be fast and flexible in order to maintain design productivity. These tools should guide the design's electrical integrity continuously, without major compromises to design performance, power, or area.The final sign-off phase requires an integrated tool suite that is production-proven and validated against real silicon.

Nanometer sign-off tools used during this phase should be more thorough and accurate than the design closure tools used during implementation. This full-chip examination should include analysis of the subtle and complex interactions that occur between many different electrical effects across many process corners. For example, nanometer sign-off should predict how IR drop affects crosstalk—and how this affects timing, which in turn affects power, which is responsible for IR drop. The key components of nanometer sign-off include accurate 3-D parasitic extraction, full-chip IR drop analysis, full-chip crosstalk analysis, and SI-aware static timing analysis (STA) that accounts for the influence of both crosstalk and IR drop.

III. 3-D PARASITIC EXTRACTION

Extraction accuracy is largely a function of the relationship between the tool vendor and the foundry and also a function of the design representation. Tool vendors need early access to proprietary process information to determine how best to model the process and to capture the necessary process characteristics. Tools need to use the physical details of design elements, rather than simplistic abstractions. As an example, while it is expedient to provide a simplified model of a port, doing so inherently limits design optimization. Similarly, cell models should be instance-specific, not treated as if each cell were isolated.

From a methodology point of view, getting the most out of the silicon requires utilizing the most accurate necessary physical information for design iterations. For early design iterations, turnaround time is important and later in the design cycle, accuracy is most critical issue. Using a less accurate extractor to speed iterations can mean increased margin and increased timing closure risk. An extractor should be fast enough to enable designers to complete block iterations within 1-2 hours. It should also complete a full-chip extraction overnight, using multiprocessor computers if necessary to do so. The output from 3-D extraction tools is either a parasitic database or a text file in detailed specified parasitic format

(DSPF) or standard parasitic extraction format (SPEF). SPEF is required for coupling extraction, which is critical for accurate SI analysis. As design sizes increase, so do the number of parasitic elements required for accurate analysis.

IV. IR DROP ANALYSIS

IR drop due to parasitic effects, such as resistance or capacitance, cause a decrease in the current flowing from the VDD (source) input/output pins to the transistors or gates of a design. **An excessive IR-drop can increase the delay of targeted paths (global effect)** and significantly reduce the voltage reaching a device causing reason for logic failure.

The risk of IR drop increases with the shrinking process technologies of nanometer design. With each new generation of process technology, the current demand per unit area of a design is increased due primarily to shrinking gate-oxide thickness. This, combined with the fact that nanometer designs contain more transistors or gates, adds additional stress to power grid integrity.

The effect of IR drop on chip performance is significant, primarily affecting timing. IR drop compromises the drive capability of the gates and increases the overall delay. Typically, a 5% drop in supply voltage can affect delay by 15% or more. Such an increase in delay is critical when clock skews are in the range of 100 picoseconds. IR drop can make path delay unpredictable and can even cause the critical path of a design to change. For this reason, nanometer timing calculations must take IR drop into account.

IR drop has significant impact on SI. Supply voltages shrink as nanometer device dimensions are scaled to avoid transistor punch-through conditions, hot-electron effects, and device breakdown. This has resulted in smaller and smaller noise margins. IR drop reduces these margins even further, rendering nanometer designs more vulnerable to SI noise effects.

A complete picture of power grid integrity can only be obtained when effects such as IR drop, ground bounce, and electro migration are computed and analyzed accurately. These effects involve complex interactions across a chip and must be analyzed at the full-chip level. However, a leading-edge 45 nm design can contain over 10 million gates, processed with eight layers of metal, which could produce a VDD grid approaching one billion RC elements.

Therefore, power grid verification tools must have the capacity and performance required to analyze detailed representations of such large, complex chips with reasonable turnaround time.

Many power grid verification tools rely on oversimplifications, such as black-boxing embedded IP blocks or using simple power-consumption distribution models, thus trading accuracy for speed. However, because the current flowing through a chip's power grid doesn't stop at the ports of cells and IP blocks, power grid verification tools must be accurate to the transistor level while maintaining the speed and

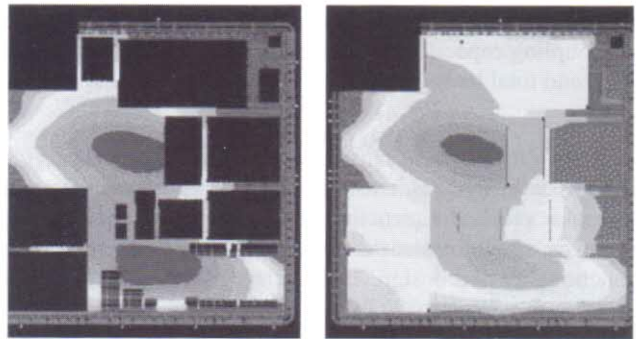

Fig. 3 Gate-level analysis doesn't accurately model IP.

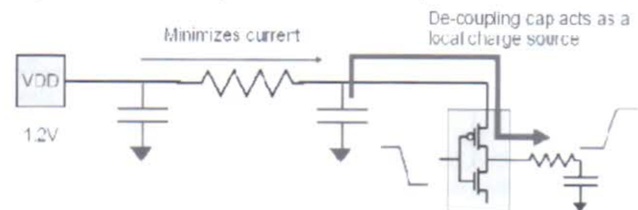

Fig. 4 Shrinking design impact IR drop analysis.

efficiency required for large-scale nanometer designs, as shown in Figure 3. The ability to pre-characterize the power grids of library elements facilitates the reuse strategies that are central to nanometer design styles.

In the gate-level plot (left), the IR drop in the center of the chip is fairly severe. But the transistor-accurate analysis (right) of the IP's contents and the current flowing through the IP reveals that the IR drop is actually much smaller

We need to understand General robustness of power rail design (static), Power rail electro migration (static), IR drop impact on timing (dynamic),Optimal size & location of de-coupling capacitance (dynamic),Trade-off de-coupling capacitance vs leakage power (dynamic)

This figure 4 shows how de-coupling capacitors are added to the power rails to minimize IR drop transients. What happens is that the de-coupling capacitor acts as a local charge source to help charge up the load capacitor through the p-channel transistor. This local charge source helps to minimize the amount of current that is drawn through the resistive power rails, which helps minimize IR drop transients.

To understand the general robustness of the power rails, a static approach can be used. This approach will clearly identify major weaknesses in the power rails, such as routing that is too narrow and missing vias or power straps. The value of the static approach is that it is available very early in the design cycle, even prior to signal routing being completed.

The static approach is also the best solution for power rail electro migration, since electro migration is caused by high average currents flowing over a period of time.

The static approach is good down to 130nm, but beyond 130nm, a dynamic approach should be used so that the impact